

Serial No. 09/605,293
Atty. Docket No. MIO 0037 VA

At page 13, lines 17-28 should read:

D5
After the insulating substrate 202 has been doped with hydrogen ions, the layer 204 of semiconducting material 206 is formed on the substrate 202 by any conventional deposition process. Useful deposition methods include, but are not limited to, CVD, LPCVD, PECVD, MOCVD and sputtering. The layer 204 of semiconducting material 206 can be any material used to form semiconducting layers, including, but are not limited to, gallium arsenide, indium phosphide, polycrystalline silicon, and germanium. Desirably, the layer 204 of semiconducting material 206 is formed from polycrystalline silicon. Once the layer 204 of semiconducting material 206 has been formed, the layer 204 is etched to isolate the various regions of semiconducting material from each other on the surface of the substrate 202.

At page 14, lines 12-18 should read:

D6
As a final step, a layer 216 of a conducting material 218 is formed on the layer 212 of dielectric material 214. The layer 216 is formed in any manner currently used in the art to form such layers. Useful deposition methods include, but are not limited to, CVD, LPCVD, PECVD, MOCVD and sputtering. The conducting material 218 is selected from the group consisting of polycrystalline silicon, metal, and any conducting material. The layer 216 of conducting material 218 forms the gate electrode 220.

In the Claims

D7N
10. (Thrice Amended) A field effect transistor comprising:

- a semiconductor substrate;
- a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

Serial No. 09/605,293
Atty. Docket No. MIO 0037 VA

a layer of polycrystalline silicon formed on at least a portion of said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology; and

a gate oxide formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

D7 a source and a drain formed in said semiconductor substrate with a gate electrode formed on said semiconductor substrate from said layer of polycrystalline silicon to form a field effect transistor.

11. (Thrice Amended) A memory array comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor; [and]

a gate oxide for each of said field effect transistors formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source and a drain for each of said field effect transistors formed in said semiconductor substrate; and

a gate electrode for each of said field effect transistors formed on said semiconductor substrate from said layer of polycrystalline silicon.

12. (Thrice Amended) A semiconductor wafer comprising:

Serial No. 09/605,293
Atty. Docket No. MIO 0037 VA

a wafer including a semiconductor substrate, said wafer being divided into a plurality of die;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, on each of said plurality of die said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

D7 a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a repeating series of gate oxides formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a repeating series sources and drains for at least one field effect transistor formed in each of said plurality of die, said series of gate oxides, sources and drains being formed in said semiconductor substrate; and

a repeating series of gate electrodes for at least one field effect transistor formed on each of said plurality of die, said series of gate electrodes being formed on said semiconductor substrate from said layer of polycrystalline silicon.

14. (Thrice Amended) A thin film transistor comprising:

D8 a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass, said semiconductor substrate having hydrogen ions implanted therein by plasma source ion implantation, wherein said semiconductor substrate is free of metal contaminants;

a layer of polycrystalline silicon formed on at least a portion of semiconductor substrate, said layer of polycrystalline silicon having a smooth morphology;

a layer of an insulating material formed on at least a portion of said layer of polycrystalline silicon;